

FIG. 1

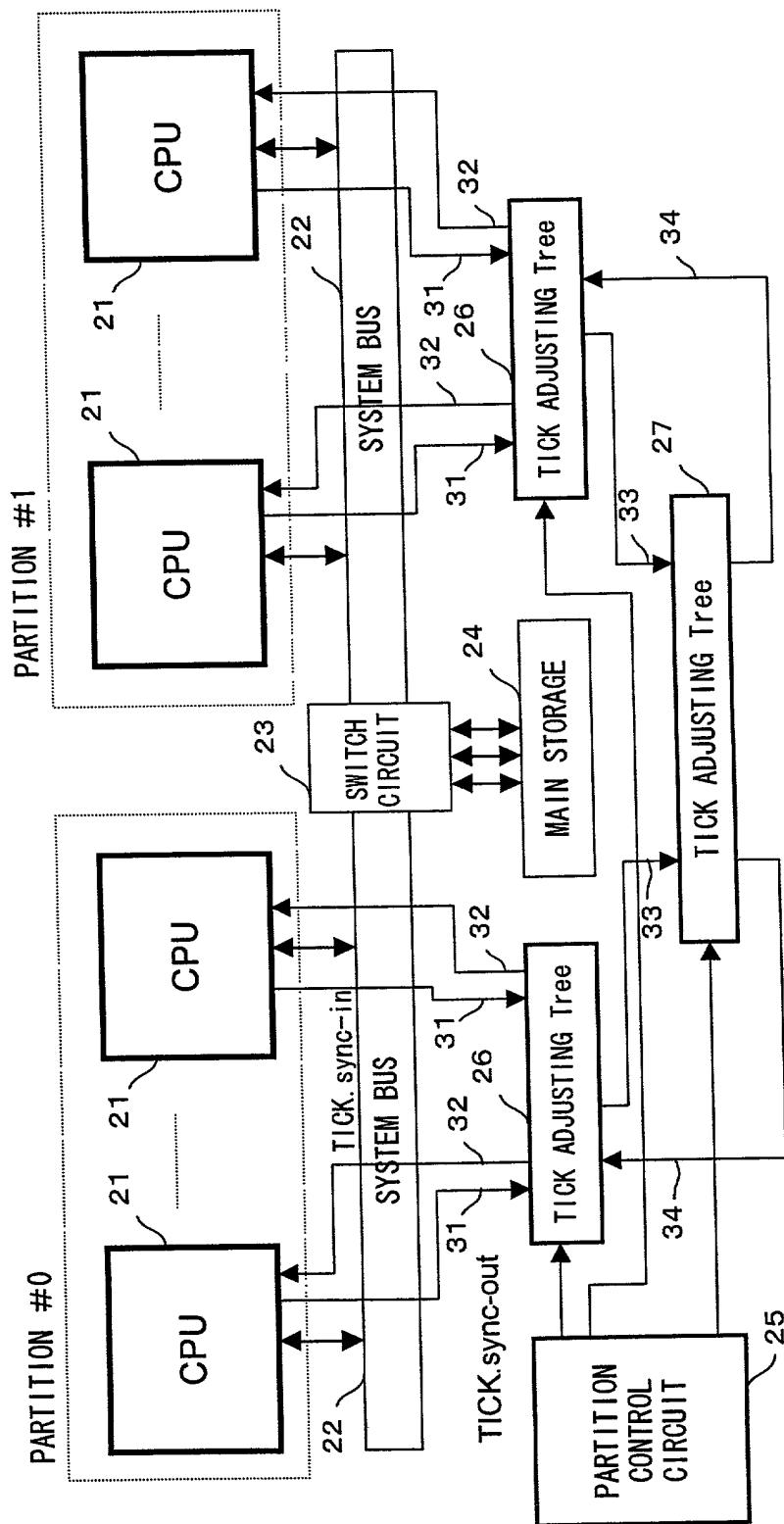


FIG. 2



FIG. 4 is a block diagram of a system architecture showing a series of CPUs (CPU #0 to CPU #7) connected to a common bus system. Each CPU is connected to a local OR gate (61) which is part of a larger OR gate assembly (62, 63). The outputs of these OR gate assemblies are connected to a common bus (64) which is then connected to a memory unit (65). The memory unit is shown as a stack of three memory modules (2, 1, 0) with a control line (65) and a data line (64).

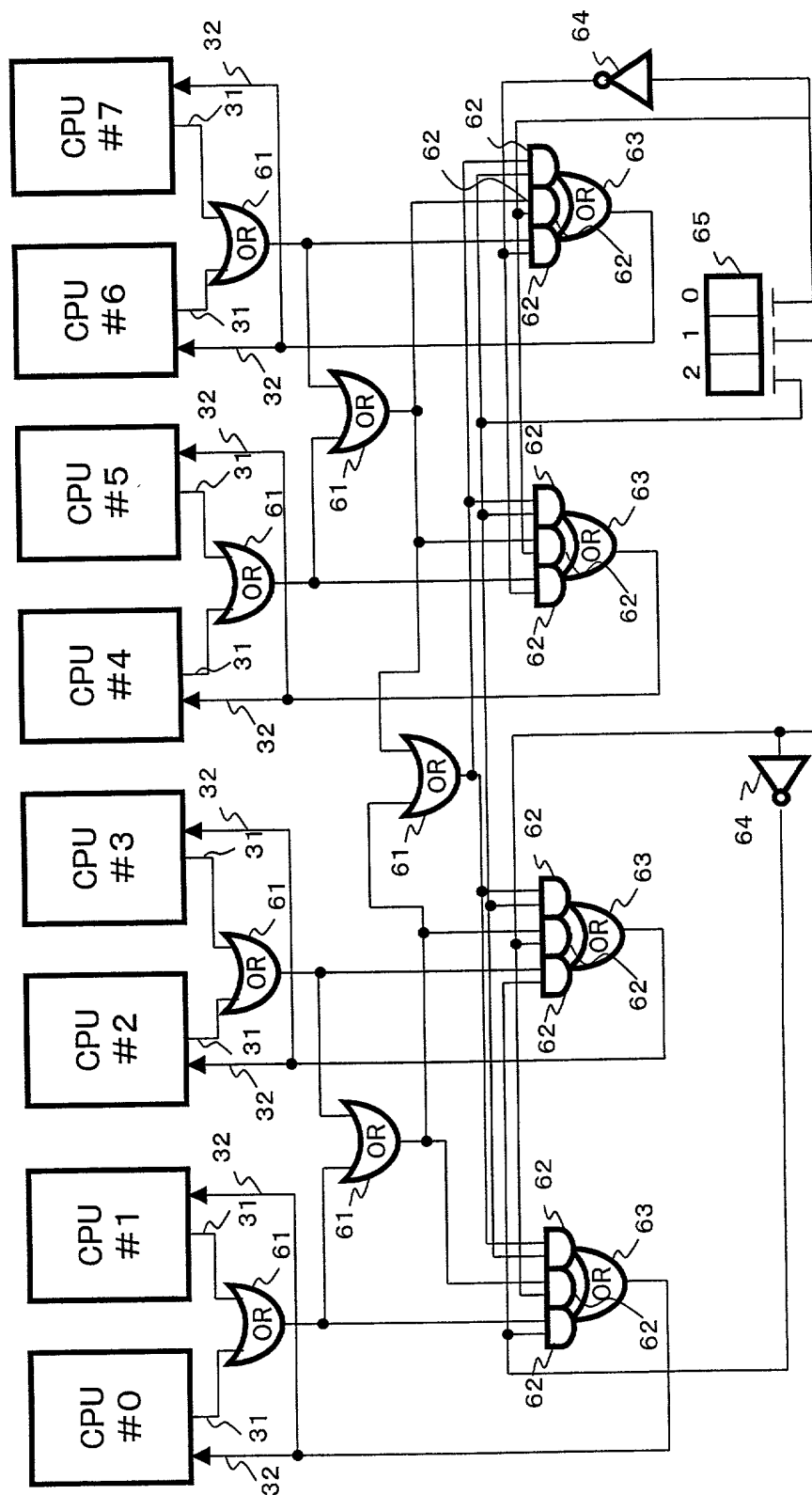


FIG. 4

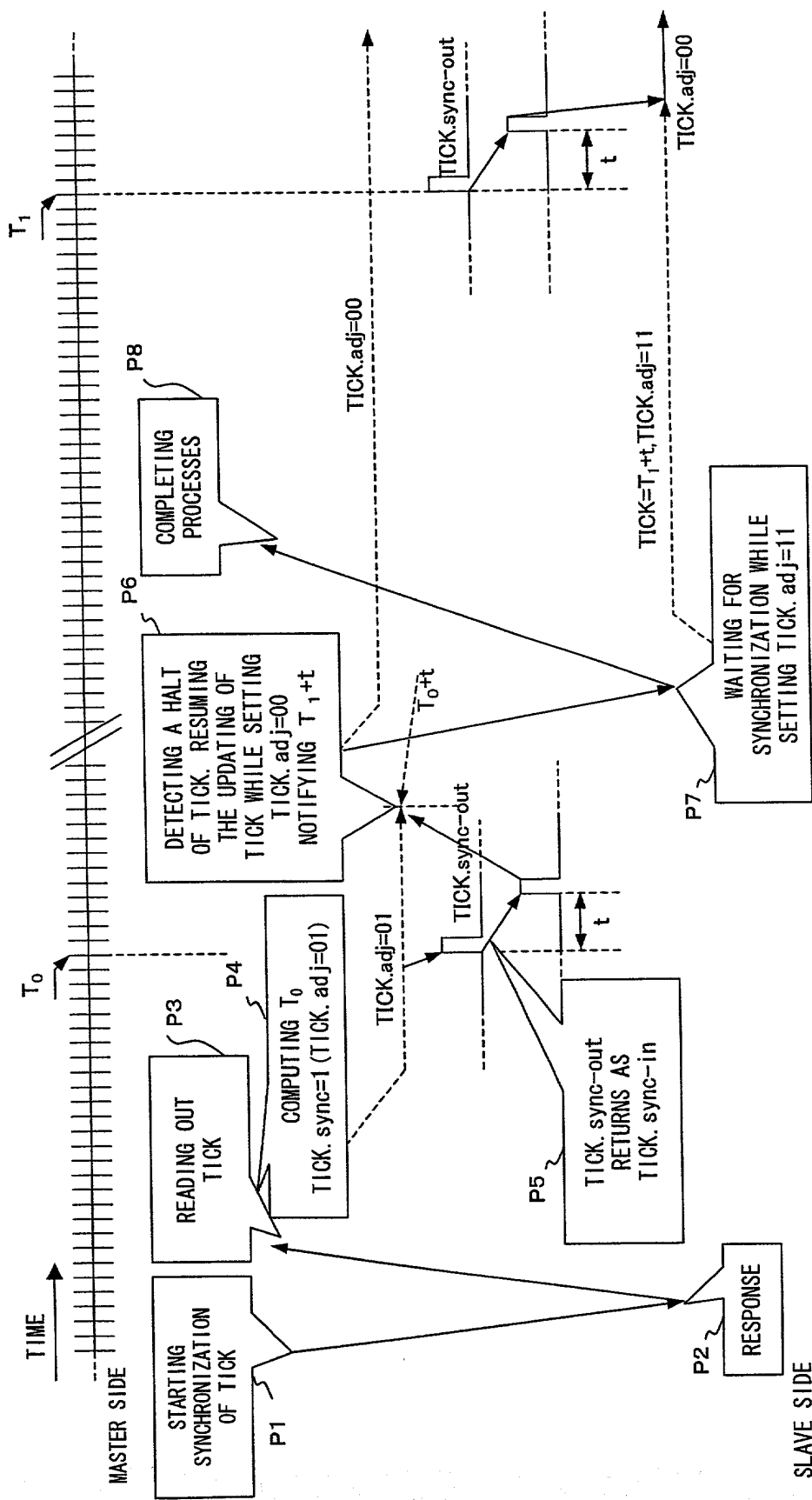


FIG. 5

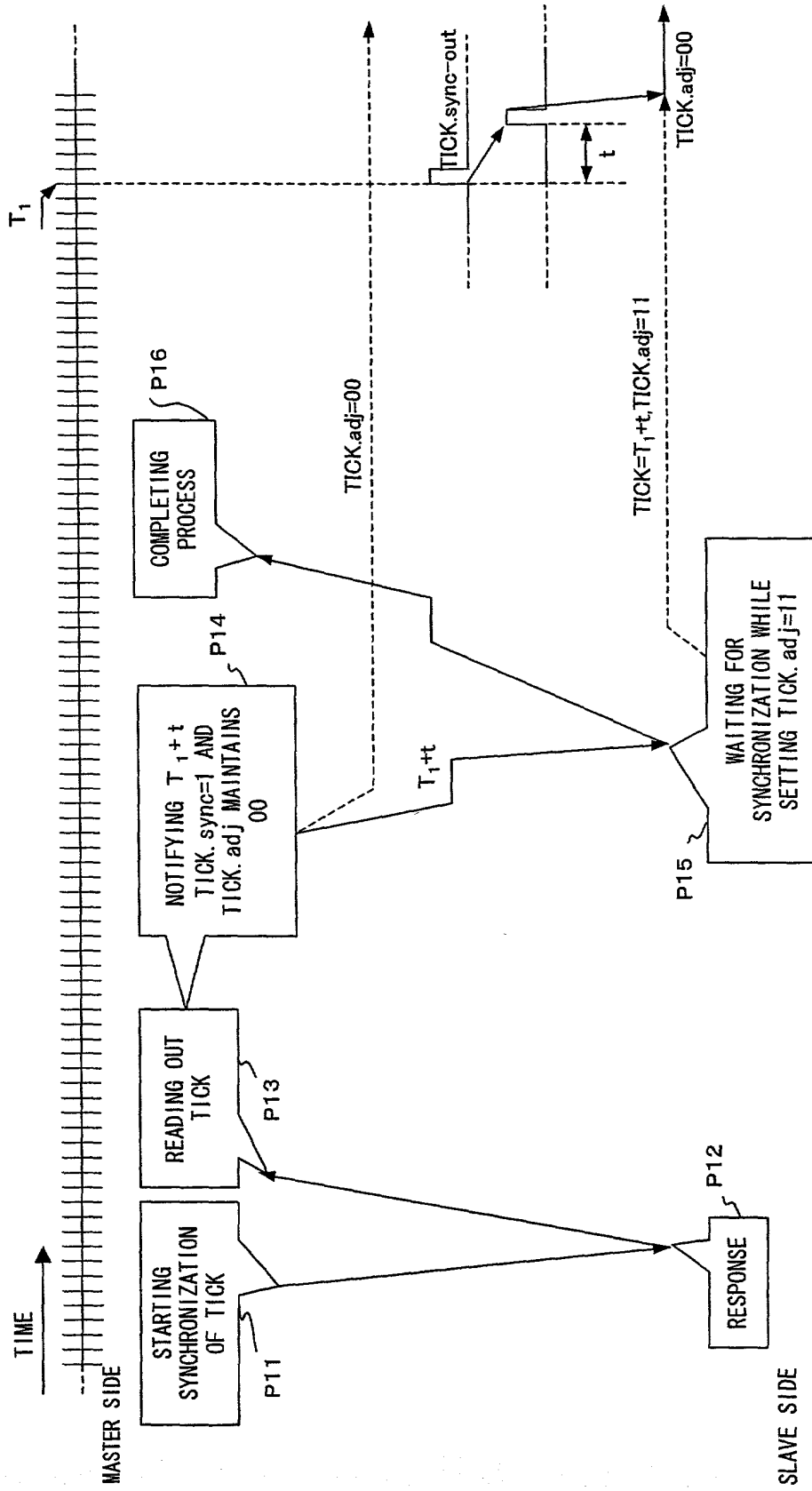


FIG. 6